1. (Amended) An integrated circuit having logic blocks comprising

a control unit for performing test and debug operations of said logic blocks of said integrated circuit;

a memory associated with said control unit, said memory holding instructions for said control unit; and

[a plurality of scan lines responsive to said control unit for loading test signals for said logic blocks and retrieving test signal results from said logic blocks, said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed at one or more clock signal rates internal to said integrated circuit] a plurality of probe lines responsive to said control unit for carrying system operation signals at predetermined probe points of said logic blocks, said system operation signals stored in said memory so that said system operation signals are retrievable.

2. (Amended) The integrated circuit of claim 1 further comprising

[a plurality of probe lines responsive to said control unit for carrying system operation signals at predetermined probe points of said logic blocks, said system operation signals stored in said memory so that said system operation signals are retrieved at one or more clock signal rates internal to said integrated circuit] a plurality of scan lines responsive to said control unit for loading test signals for said logic blocks and retrieving test signal results from said logic blocks, said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed at one or more clock signal rates internal to said integrated circuit.

3. (Amended) The integrated circuit of claim [1] 2 further comprising

a unit coupled to said control unit and said memory, said unit testing said logic blocks and said memory responsive to and in cooperation with said control unit to self-test said integrated circuit.

4. (Amended) The integrated circuit of claim [1] 2 wherein said scan lines comprise a first string of flip-flop connectors connected between a logic block and the remainder of said integrated circuit proximate said logic block, said flip-flop connectors

providing signal paths between said logic block and the remainder of said integrated circuit proximate said logic block in one mode and carrying test signals and test signal results in a second mode.

5. (Amended) The integrated circuit of claim [1] 2 wherein said scan lines comprise a second string of flip-flop connectors between elements of a logic block, said flip-flop connectors providing signal paths between said logic block elements in one mode and carrying test signals and test signal results in a second mode.

6. (Amended) The integrated circuit of claim [2] 1 wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points of said logic blocks in one mode.

7. (As filed) The integrated circuit of claim 6 wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode.

8. (As filed) The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying digital state system operation signals.

9. (As filed) The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals reflective of analog conditions at said predetermined probe points.

10. (Amended) An integrated circuit comprising

an interface for coupling to an external diagnostic processor;

a unit responsive to instructions from said external diagnostic processor for capturing [sequential of] sets of sequential system operation signals of said integrated circuit;

a plurality of probe lines coupled to said unit for carrying said system operation signals at predetermined probe points of said integrated circuit;

a memory coupled to said unit and to said interface, said system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit [;

whereby] so that said external diagnostics processor can process said captured system operation signals.

11. (Amended) The integrated circuit of claim 10 wherein said unit further comprises trigger logic responsive to said system operation signals for initiating storage of a set of said system operation signals in said memory.

12. (Amended) The integrated circuit of claim 11 wherein said trigger logic is responsive to said system operation signals for terminating storage of said set of said system operation signals in said memory.

13. (As filed) The integrated circuit of claim 10 wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points in one mode.

14. (As filed) The integrated circuit of claim 13 wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode.

15. (Amended) A method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of [scan] probe lines of said logic blocks, said method comprising

[loading said memory with test signals and instructions for said control unit;

loading said scan lines responsive to said control unit with said test signals for said logic blocks at one or more clock signal rates internal to said integrated circuit;]

operating said logic blocks to perform system operations at one or more clock signal rates internal to said integrated circuit;

enabling said probe lines responsive to said control unit to capture system operation signals of said logic blocks at one or more clock signal rates internal to said integrated circuit;

retrieving [test signal results] said system operation signals from said logic blocks along said [scan] probe lines at one or more clock signal rates internal to said integrated circuit,

storing said [test signal results] system operation signals in said memory at one or more clock signal rates internal to said integrated circuit; and

processing said [stored test results] stored system operation signals [in said control unit responsive to said stored instructions in said memory] to perform test and debug operations of said logic blocks of said integrated circuit.

Add new claims 16-22 as follows:

16. (New) The method of claim 15 wherein said system operation signals comprise sequential system operation signals.

17. (New) The method of claim 16 wherein said system operation signals comprise sets of sequential system operation signals.

18. (New) The method of claim 15 wherein said integrated circuit has a plurality of scan lines of said logic blocks, said method further comprising

loading said memory with test signals and instructions for said control unit;

loading said scan lines responsive to said control unit with said test signals for said logic blocks at one or more clock signal rates internal to said integrated circuit;

operating said logic blocks at one or more clock signal rates internal to said integrated circuit;

retrieving test signal results from said logic blocks along said scan lines at one or more clock signal rates internal to said integrated circuit,

storing said test signal results in said memory at one or more clock signal rates internal to said integrated circuit; and

processing said stored test results signals in said control unit responsive to said stored instructions in said memory to perform test and debug operations of said logic blocks of said integrated circuit.

19. (New) The integrated circuit of claim 10 wherein said memory is also coupled to said system operation unit so that said memory unit may be accessed selectively or simultaneously by said data capture unit and said system operation unit.

20. (New) The method of claim 1 wherein said system operation signals comprise sequential system operation signals.

21. (New) The method of claim 20 wherein said system operation signals comprise sets of sequential system operation signals.

22. (New) The method of claim 1 wherein said system operation signals are stored in said memory at one or more clock signal rates internal to said integrated circuit.

REMARKS

Reconsideration of the present patent application, as amended, is respectfully requested.

Of previously pending claims 1-15, all were rejected. Claim 10 was rejected under 35 USC §112, second paragraph, for indefiniteness. The applicants have amended claim 10 accordingly.

Substantively, claims 1, 3-5, and 15 were rejected under 35 USC §103(a) as being obvious over the combination of U.S. Patent No. 5,991,898, which issued November 23, 1999 to J. Rajki *et al.* and U.S. Patent No. 6,003,142, which issued December 14, 1999 to J. Mori. Claims 2 and 6-9 were rejected under 35 USC §103(a) as being obvious over the combination of the cited Rajki and Mori patents and further in view of U.S. Patent No. 5,202,624, which issued April 13, 1993 to T.R. Gheewala *et al.* The balance of the claims, i.e., claims 10-14, were rejected under 35 USC §103(a) as being obvious over the combination of the cited Mori and Gheewala patents.